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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/062,992	01/31/2002	Steven Teig	SPLX.P0096	2859

7590 01/21/2005

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EXAMINER	
LU, KUEN S	

ART UNIT	PAPER NUMBER
2167	

DATE MAILED: 01/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/062,992	TEIG ET AL.	
	Examiner	Art Unit	
	Kuen S Lu	2167	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1-7/1/04,2-11/1/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED

Response to Amendments

1. The Action is responsive to the Applicant's Amendments, filed on November 1, 2004. The amendment made to the specifications and drawings is noted and considered. Also noted and considered is the two Information Disclosure Statement by Applicant, submitted on July 1, 2004 and November 1, 2004, respectively.

2. In responding to Applicant's Remarks, the Examiner has created this Office Action for Final Rejection (hereafter "the Action") as shown next. Please note in the Action, the Examiner maintained the same position as set forth in the non-Final Office Action for Rejection, dated July 22, 2004.

3. As for the Applicant's Remarks on claim rejections, filed on November 1, 2004, has been fully considered by the Examiner, please see discussion in the section ***Response to Arguments***, following the Office Action for Final Rejection.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U. S. C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-19 are rejected under U. S. C. 102(b) as anticipated by Pedersen et al. (U. S. Patent 6,134,705, hereafter "Pedersen").

As per claim 1, Pedersen teaches the following:

"A data storage structure that stores a plurality of sub-networks," at col. 11, lines 44-60 where newly and original synthesized sub-netlist are saved, and "wherein each sub-network performs an output function" at col. 11-14 and Figs. 7A-7F, nodes u and v, where sub-netlists perform output functions. Further, Pedersen teaches "wherein the data storage structure stores each sub-network based on a parameter derived from the output function of the sub-network" at Figs. 7E-7F and col. 16, lines 21-39 where the un-synthesized sub-netlist Fig. 7E performs output functions at nodes u and v, and Fig. 7F is the parameter derived at the synthesized sub-netlist is at node u.

As per claim 2, Pedersen teaches "some of the sub-networks are multi-function sub-networks, wherein each multi-function sub-network performs more than one output function, wherein the parameter of each multi-output function is derived from all the output functions of the multi-output function" at Figs. 7E-7F and col. 16, lines 21-39 where the un-synthesized sub-netlist Fig. 7E performs output functions at nodes u and v, and the parameter derived at the synthesized sub-netlist Fig. 7F is at node u.

As per claim 3, Pedersen teaches "each sub-network includes a set of circuit elements, and the data storage structure stores each sub-network in terms of (i) a graph that represents the topology of the set of circuit elements of each sub-network, wherein the graph includes a node for each circuit element of the sub-network, (ii) a set of local functions that includes a local function for each node of the graph" at Fig. 7A and at col. 1, lines 37-44 where the sub-netlist (element 700) includes elements 702-740, and Southgate (referenced by Pedersen at col. 1, lines 37-43) states a fully described block

diagram stored in a graphic design file at col. 4, lines 65-67, and further at Fig. 7E where a set of local functions include the functions at nodes u and v.

As per claim 4, Pedersen teaches "the data storage structure stores, for each sub-network, an identifier that specifies the set of local functions and the graph that specify the sub-network" at col. 11, line 62 – col. 4, line 3 where a sub-netlist is identified and synthesized for its nodes and the graph by mapping the changed design onto the target hardware.

As per claim 5, Pedersen teaches "the identifier for each sub-network specifies the locations that store the set of local functions and the graph of the particular sub-network" at Figs. 4A-4B and at col. 11, line 62 – col. 4, line 3 where a sub-netlist is identified and synthesized for its nodes and the graph by mapping the changed design onto the target hardware.

As per claims 6 and 16, Pedersen teaches "the identifier for each sub-network is a set of indices that specifies the set of local functions and the graph of the sub-network" at Figs. 4A-4B and col. 11, lines 62-66, col. 12, lines 10-15 and 43-45, and col. 13, lines 28-38 and 43-54 where an identified sub-netlist is analyzed for its gates locations and nodes functions.

As per claims 7 and 17, Pedersen teaches "the set of indices for each sub-network includes a graph index and a set of function indices, wherein, for each sub-network, the graph index identifies the storage location of the graph for the sub-network, and each function index identifies the storage location of a local function of the sub-network" at

Figs. 4A-4B and col. 6, lines 29-35 and 54-59 where gates and nodes are selected from the synthesize and un-synthesized sub-netlist one by one for analysis.

As per claims 8 and 18, Pedersen teaches "the storage structure is a database, and the graphs are stored in a graph table, the local functions are stored in at least one function table, wherein each graph index specifies a record in the graph table, and each function index specifies a record in the function table" at Fig. 7A and col. 1, lines 37-44 and Southgate: at col. 9, lines 28-36 and 41-49 where graphic editor uses graphic design database for reading from writing to the graphic design block diagram for integrated circuit and interacts with hierarchy information database which stores the hierarchy information files for each IC design.

As per claims 9 and 19, Pedersen teaches "the local functions are stored in multiple function tables, wherein a first function table is for are n-input functions, and a second function table is for m-input functions, where n and m are integers, wherein some of the function indices specify functions in the first function table while other function indices specify functions in the second function table" at Fig. 7D where sub-netlists 762, 764 and 766 each has two inputs and one output functions while 776 has four and two, respectively.

As per claim 10, Pedersen teaches "the data storage structure associates the generated parameter for each sub-network with the graph and function identifier for the sub-network" at col. 11, line 62 – col. 4, line 3 where a sub-netlist is identified and synthesized for its nodes and the graph by mapping the changed design onto the target hardware.

As per claim 11, Pedersen teaches the following:

"a data storage structure that stores a plurality of sub-networks, wherein each sub-network performs an output function" at col. 11, lines 44-60 where newly and original synthesized sub-netlist are saved, and sub-netlists perform output functions (at col. 11-14 and Figs. 7A-7F, nodes u and v), further, Pedersen teaches "wherein the data storage structure stores each sub-network based on a parameter derived from the output function of the sub-network" at Figs. 7E-7F and col. 16, lines 21-39 where the un-synthesized sub-netlist (Fig. 7E) performs output functions at nodes u and v, and the parameter derived at the synthesized sub-netlist is at node u (fig. 7F); and

"a data access manager that identifies and retrieves sub-networks from the data storage structure" at Fig. 3A, step 314, and col. 10, lines 40-50 where compiler is the data access manager for identifying the sub-netlist, by a comparison process, and retrieving the sub-netlist to be incrementally recompiled.

As per claim 12, Pedersen teaches "the data access manager receives a parameter, the manager searches the data storage structure for sub-networks that are stored based on the received parameter, and if the manager finds a sub-network that is stored based on the received parameter, the manager retrieves the sub-network" at Fig. 3A, step 314, and col. 10, lines 43-50 where user input the changed design for receiving and retrieving the sub-netlist to be incrementally recompiled.

As per claim 13, Pedersen teaches the following:

"each sub-network includes a set of circuit elements, and the data storage structure stores each sub-network in terms of (i) a graph that represents the topology of the set of

circuit elements of each sub-network, wherein the graph includes a node for each circuit element of the sub-network, (ii) a set of local functions that includes a local function for each node of the graph" at Fig. 7A and at col. 1, lines 37-44, for example, the sub-netlist (element 700) includes elements 702-740 and Southgate (referenced by Pedersen at col. 1, lines 37-43) stated a fully described block diagram is stored in a graphic design file at col. 4, lines 65-67, and further at Fig. 7E where a set of local functions include the functions at nodes u and v; and

"for each retrieved sub-network, the manager retrieves the graph and the set of local functions of the sub-network" at Fig. 3A, step 314, and col. 10, lines 40-50 where compiler is the data access manager for identifying the sub-netlist, by a comparison process, and retrieving the sub-netlist to be incrementally recompiled.

As per claim 14, Pedersen teaches the following:

"the data storage structure stores, for each sub-network, an identifier that specifies the set of local functions and the graph that specify the sub-network" at col. 11, line 62 – col. 4, line 3 where a sub-netlist is identified and synthesized for its nodes and the graph by mapping the changed design onto the target hardware;

"the data storage structure associates the generated parameter for each sub-network with the graph and function identifier for each sub-network" at Fig. 3A, step 314, and col. 10, lines 40-50 where the compiler conducts a the process for identifying the sub-netlist, by a comparison process, and retrieving the sub-netlist to be incrementally recompiled; and

"the manager uses the received parameter to identify an identifier associated with the received parameter, and then uses the identified identifier to retrieve a graph and a set of local functions" at Fig. 3A, step 314, and col. 10, lines 40-50 where user is allowed to input changed design for identifying the new gates such the incremental synthesized process can start.

As per claim 15, Pedersen teaches "the manager uses the received parameter to identify a set of identifiers associated with the received parameter, and then use the identified set of identifiers to retrieve graphs and sets of local functions that specify several sub-network" at Fig. 3A, step 314, and col. 10, lines 40-50 where compiler is the data access manager for identifying the sub-netlist, by a comparison process, and retrieving the sub-netlist to be incrementally recompiled.

6. The prior art made of record

A. U. S. Patent No. 6,134,705

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

B. U. S. Patent No. 6,110,223

C. U. S. Patent No. 6,102,964

D. U. S. Patent No. 5,201,046

E. U. S. Patent No. 5,440,720

Response to Arguments

7. The Applicants' arguments filed on November 1, 2004 have been fully considered but they are not persuasive, for the Examiner's response, please see discussion below.

In the Remarks, filed on November 1, 2004, concerning the independent claims 1 and 19, the Applicant argued that the Pedersen reference does not teach "storing a sub-network in a data storage based on a derived parameter".

As to the above arguments, the Examiner respectfully disagreed. Please note the Pedersen reference teaches inserting synthesized sub-netlist into a netlist to form a new netlist and differencing the new netlist from the original by identifying the changed nodes. Based on this description, the output of netlist synthesis process is always stored such that it may serve as a base to create a new netlist and to differentiate it from the newly created. For details, please refer to column 16, lines 16-20.

8. As to dependent claims 2-10 and 12-19, which depend on claims 1 and 11, respectively, the Examiner applies the above stated arguments for the respective claim upon which they depend.

11. In light of the forgoing arguments, the 35 U.S.C ξ 102 rejections for Claims 1-19 is hereby sustained.

Conclusion

9. THIS ACTION IS MADE FINAL.

The Applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. The prior art made of record, listed on form PTO-892, and not relied upon, if any, is considered pertinent to applicant's disclosure.

If a reference indicated as being mailed on PTO-FORM 892 has not been enclosed in this action, please contact Lisa Craney whose telephone number is 571-272-3574 for faster service.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kuen S Lu whose telephone number is 571-272-4114. The examiner can normally be reached on 8 AM to 5 PM, Monday through Friday.
If at tempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Breene can be reached on 571-272-4107. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.
Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Kuen S. Lu
Patent Examiner
January 17, 2005

Luke Wassum
Primary Examiner
January 17, 2005